REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

No new matter has been introduced by any of the above amendments.

Respectfully submitted,

Lois D. Cartier
Agent for Applicants
Reg. No. 40,941

I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231, on November 12, 2002

Pat Slaback
Name

Pat Slaback
Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

21. (New) A system, comprising:

first and second bus masters;

first and second slaves;

a bus coupled to the first and second bus masters and the first and second slaves; and

a bus arbiter coupled to the bus, the bus arbiter comprising:

at least one port coupled to receive bus request commands for a transaction from either the first or second bus master and coupled to receive an address or identity of the first and second slaves for the transaction, and also coupled to communicate over the bus; and

logic circuitry that defines logic to select a bus frequency for the requested transaction.

22. (New) The system of Claim 21, wherein the logic circuitry defines logic to select a bus frequency according to the identity of the slave for the requested transaction.

23. (New) The system of Claim 21, wherein the logic circuitry defines logic to select a bus frequency according to the identity of the master for the requested transaction.

24. (New) The system of Claim 21, wherein the logic circuitry defines logic to select a bus frequency according to the length of the bus between the first or second master and the first or second slave according to which ones are involved in the requested transaction.

25. (New) The system of Claim 21, wherein the bus arbiter is processor-based.

26. (New) The system of Claim 21, wherein the bus arbiter comprises one of a group of technologies consisting of: application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and FPGAs that include embedded core processors and embedded ASIC circuitry.

27. (New) The system of Claim 26, wherein the bus arbiter includes dedicated hardware logic that performs table lookup and arbitration tasks.

28. (New) The system of Claim 21, wherein the first slave comprises:

at least one input port for receiving communication signals and control signals from the bus;

circuitry for determining a bus frequency;

circuitry for determining a ratio between an internal clock of the bus slave and the bus frequency; and

circuitry for determining when to latch communication signals being received over the at least one input port.

29. (New) The system of Claim 28, wherein:

the circuitry for determining when to latch communication signals includes a state machine; and

the state machine generates a sample cycle signal that prompts the slave to latch the communication signals.

30. (New) A system, comprising:

a port;

a bus;

a bus master coupled between the port and the bus;

a processor coupled to the bus; and

a memory device coupled to the bus,

wherein the memory device comprises a memory portion storing data that defines arbitration logic for the bus.

31. (New) The system of Claim 30, wherein the data comprises computer instructions for the processor.

32. (New) The system of Claim 30, wherein the memory device further comprises a memory portion storing computer instructions for the processor that define ordinary operation of the system.

33. (New) The system of Claim 30, wherein the system comprises at least one of a group of technologies consisting of: application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and FPGAs that include embedded core processors and embedded ASIC circuitry.

34. (New) The system of Claim 30, wherein portions of the system are implemented using dedicated hardware logic.